V. Conclusion

Short channel silicon MOSFET's have been shown to be useful in the 2- to 6-GHz frequency band. The noise behavior is slightly better than that of a 1-μm Si-MESFET and equal to a 0.5-μm Si-MESFET up to 6 GHz. The optimum noise figure is 3–3.5 dB at 3.5 GHz. The maximum frequency of oscillation is of the order of 10 GHz, and model calculations showed f_{max} values of 13 GHz to be achievable by avoiding gate overlap. The Si-MOSFET's are more linear than recessed gate and buried channel GaAs MESFET's. Ion implantation, used to realize normally OFF-MOSFET's, only slightly affects the RF small signal gain and noise figure of the devices.

Acknowledgment

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A 4-W 56-dB Gain Microstrip Amplifier at 15 GHz Utilizing GaAs FET's and IMPATT Diodes

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***Abstract*—Performance results and design considerations are presented for an all solid-state *Ku*-band power amplifier which is feasible for use in PM communication systems for airborne or spacecraft transmitter applications. Design emphasis is placed on high power, and high efficiency operation as well as on compact amplifier construction. A six-stage GaAs FET preamplifier and a driver and balanced power amplifier utilizing GaAs IMPATT diodes operating in the injection locked oscillator mode are discussed. For high power and efficiency Schottky-Read IMPATT's with low-high-low doping profiles are employed. For improved reliability the IMPATT's incorporate a TiW barrier metallization to retard degradation of the IMPATT's. Results of accelerated life testing of the IMPATT devices are also presented.**

I. Introduction

THE USE OF solid-state devices for efficient amplification of CW microwave signals to power levels of several watts in the *Ku*-band frequency range is now possible with GaAs IMPATT diodes and to a lesser extent with GaAs FET's. Solid-state amplifiers of this type have obvious application in a wide variety of telecommunication systems both military and commercial, but are especially important for airborne and space applications where high efficiency, high reliability, and small physical size is essential. The purpose of this paper is to present the performance results and corresponding design considerations for an all solid-state microwave amplifier utilizing GaAs FET's and GaAs IMPATT diodes which is feasible for such applications. Specifically, a 15-GHz 4-W 56-dB gain microstrip amplifier whose design is relevant to a spacecraft communications transmitter employing digital phase modulation is considered. For high power and high efficiency, GaAs Schottky–Read IMPATT's with low-high-low doping profiles operating in the injection-locked oscillator (ILO) mode are used in the power stages. The diodes incorporate a platinum Schottky barrier contact with a titanium/tungsten barrier layer for improved reliability. Since the modulation in the transmitter application

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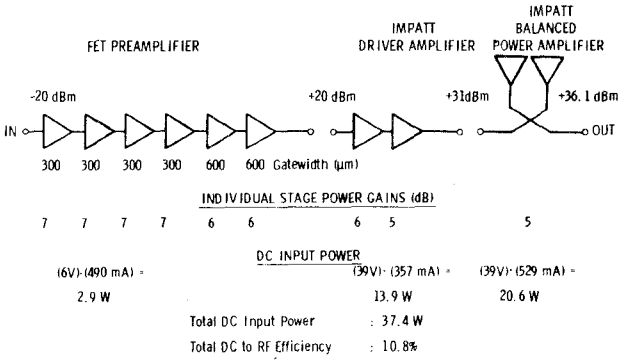


Fig. 1. Block diagram of overall amplifier.

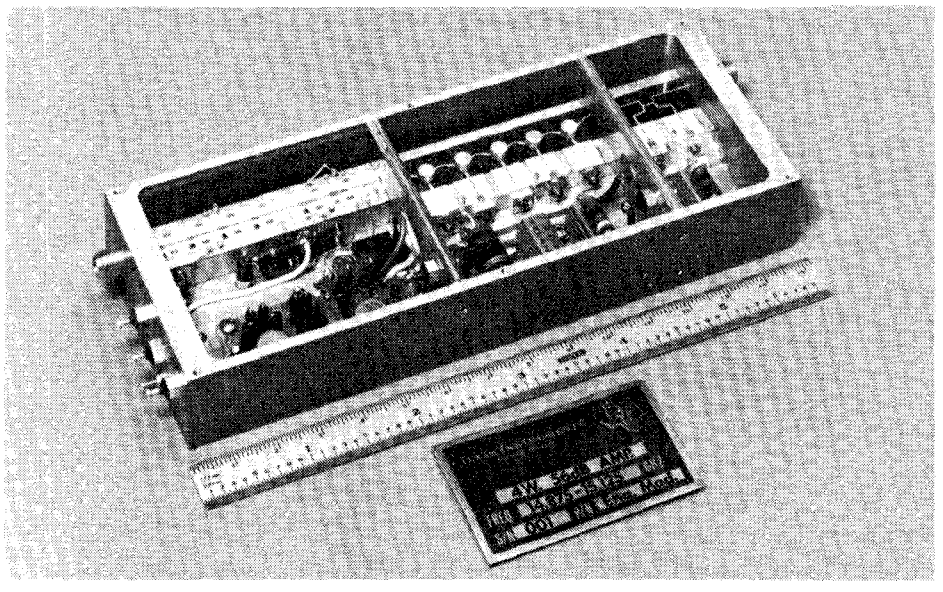


Fig. 2. Integrated amplifier and housing.

is biphase or quadrature phase-shift keying (BPSK or QPSK), the IMPATT power stages are operated in the fully power satured mode and only a limited input dynamic range is required. The GaAs FET's are used in the preamplifier which provides over 40-dB gain. The overall amplifier has a dc to RF efficiency of 10.8 percent, and operates over the 0° to 50°C temperature range with less than 0.5-dB variation in the power output over the specified operating bandwidth of 250 MHz.

II. Overall Amplifier Circuit Description

Fig. 1 shows a block diagram of the three amplifier chassis; the FET preamplifier, the IMPATT driver amplifier and the IMPATT balanced power stage. The nominal power gain of each stage as well as the dc input power and corresponding RF power output along the chain of amplifiers is also indicated. The amplifier operates from 39, 6, and -1 V commercial dc power supplies. The nominal RF input power to the amplifier ranges from threshold (< -30 dBm) to -20 dBm. Below threshold, amplification is no longer required and the driver and power amplifier stages are made idle by removing bias from the IMPATT diodes. This is accomplished automatically by means of a temperature compensated transistorized shutdown circuit which is activated by the rectified voltage of a sampling Schottky detector diode situated at the output of the FET preamplifier.

Fig. 2 shows a photograph of the integrated amplifier. It has a volume of 220 cm^3 and weighs 444 g. The input port is via the SMA connector seen at the left end of the amplifier housing. Also visible are the three bias connectors, a grounding pin and the output SMA connector at the far right. Because of the high gain of the amplifier, metal partition walls incorporating short sections of 50-Ω transmission line separate the three amplifier chassis to increase the shielding between the preamplifier and power stages. Indium metal gaskets are incorporated into the partition walls to ensure good rf grounding to the amplifier housing and the top cover plate. Included in the housing are the bias distribution circuits as well as the IMPATT shutdown circuit. The shutdown circuit utilizes a pass transistor (which switches the total IMPATT bias current) whose base current is controlled by the amplified output of a comparator. The inputs to the comparator are a voltage proportional to the Schottky detector output and a reference voltage. The reference voltage is potentiometer adjustable, thereby enabling one to set the IMPATT shutdown circuit to trigger at a specific RF input threshold level.

III. GaAs IMPATT Devices and Results of Reliability Testing

A. Fabrication and Evaluation in Waveguide [1]

The low–high–low GaAs IMPATT structures are grown in a single run by a $AsCl_3$-Ga-H_2 vapor phase epitaxial process [2]. A special feature of the epitaxial system employed here is that a small volume of doping gas can be injected into a hydrogen line with a high gas flow velocity and carried rapidly into the epitaxial deposition zone, thus producing a narrow doping spike. The epitaxial layers are sulphur doped. The whole structure consists of a highly doped buffer layer, a lower doped drift layer and, close to the surface, a narrow doping spike. After forming the doping spike, the lower doped surface layer is grown to a thickness considerably greater than required for device fabrication. Slices are then characterized to determine uniformity, and whether their parameters are within the design window for high-efficiency devices [1], [3]. For suitable slices the optimum low layer thickness (distance of Schottky barrier junction to doping spike) is determined and anodic oxidation [4] is used to thin this layer to the optimum value.

For improved reliability the IMPATT's employ a high reliability metallization system. Because of a reaction between Pt and GaAs which is known to proceed fairly rapidly [5], the Pt/GaAs interface of a Read-type, Schottky barrier GaAs IMPATT advances into the device causing reliability and performance degradation. To impede this reaction, a thin Pt contact layer followed by a refractory barrier metal is used [6]. Specifically, the front metallization (junction side) consists of 300 Å Pt/2200Å TiW (90%W by weight)/1000 Å Pt followed by a 250-μm thick Au-plated heat sink. The metallization is serially deposited by sputtering in one pump-down after a brief sputter etch of the GaAs surface.

The substrate side of the slice is prepared as follows. After substrate thinning, an AuGe/Ni back contact is evaporated and gold plated to a thickness of 1 to 2 μm. Mesas, typically 100 to 140 μm in diameter, are then etched and the back contacts alloyed at 460°C for ~1 min. The ohmic back contact is employed to counteract possible unreliability due to current crowding and resultant thermal runaway. Finally, the individual mesas are separated by sawing the Au heat sink. Devices are mounted in microwave packages for testing in a waveguide cavity employing the "tuning hat" configuration. In the oscillator mode of operation, output powers of 1.5 to 2.6 W at mid *Ku*-band with 17–23 percent efficiency were typically obtained from single mesas.

B. Microstrip Oscillator Evaluation.

The IMPATT diodes are evaluated as free-running oscillators in a microstrip test fixture shown in Fig. 3. The basic microstrip circuit consists of a 50-Ω transmission line, a 10-pF beam lead capacitor for dc blocking, and a $\lambda/4$ transformer section to reduce the real part of the impedance to ~3.6 Ω. The microstrip circuit is fabricated on 0.25-mm thick polished alumina. The diode, which has an integral plated heat sink, is alloyed onto a gold-plated copper block and attached to the microstrip circuit block with a small screw. Multiple gold bonding wires are used to connect the top of the mesa to the alumina circuit. To minimize the inductance, gold ribbon is used on the larger mesa diodes. The diode mounting scheme used in the test fixtures is identical to that employed in the final amplifier assemblies.

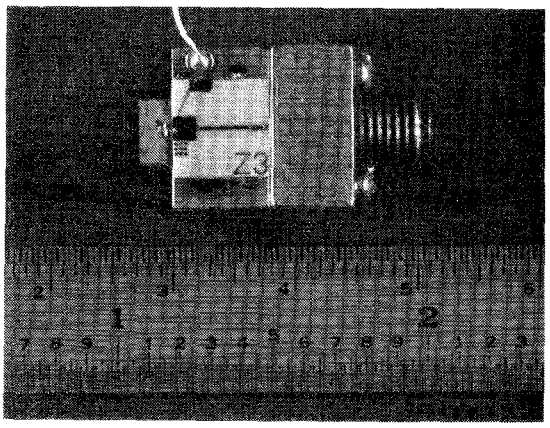
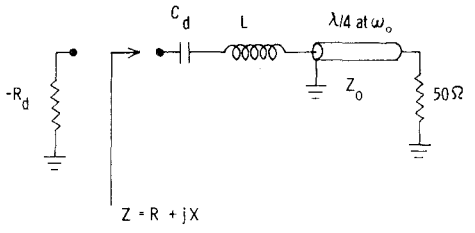


Fig. 3. Microstrip oscillator test fixture.



For stable oscillation at ω_0, $Z = R = R_d$ (magnitude of diodes negative resistance).

$$\text{Reactance Slope}\Big|_{\omega_0} = \frac{dX}{d\omega}\Big|_{\omega_0}$$

$$Q_e = \frac{\omega_0}{2R} \cdot \frac{dX}{d\omega}\Big|_{\omega_0}$$

Fig. 4. Simplified circuit for external Q calculation.

The external Q for this circuit can be approximated by considering the reactance slope at series resonance [7], [8]. Fig. 4 shows the simplified circuit for the calculation. The bond lead inductance is assumed to series resonate the diodes capacitance at 15-GHz and the $\lambda/4$ transformer to transform from 50 Ω to 3.6 Ω. The reactance slope evaluated at resonance is

$$\frac{dX}{d\omega}\Big|_{\omega_o} = 2L + \frac{\pi Z_o}{2\omega_o}\left[1 - z_o^2\right] \tag{1}$$

and

$$Q_e = \frac{\omega_o}{2R} \cdot \frac{dX}{d\omega}\Big|_{\omega_o} = \frac{\omega_o L}{R} + \frac{\pi}{4z_o}\left[1 - z_o^2\right] \tag{2}$$

where

$$z_o = \frac{Z_o}{50} \leqslant 1$$

Z_o is the characteristic impedance of the quarter-wave section (13.4 Ω), and R is the transformed resistance. A reasonable value for L, the bond lead inductance, is 0.15 to 0.25 nH. Substituting these values in (2), it is found that Q_e is about 6.6 to 10.5 at 15-GHz.

For a specific device, the oscillator circuit is optimized for maximum power output by tuning with metallized ceramic chips. Mesa diameters up to about 120 μm can be operated as oscillators at 15 GHz with output powers up to 1.8 W and 23-percent efficiency using this microstrip test fixture. The use of larger area devices and multiple mesa operation was also attempted for higher power output. However, difficulties encountered with lower impedance levels, interconnect parasitics, and generally unrepeatable results obtained with various bonding configurations, dictated the use of single mesa devices for best power and efficiency performance at 15 GHz.

C. IMPATT Reliability Investigation.

As with other investigators, we began this work under the assumption that temperature effects were dominant in causing device failure; our experiments were designed accordingly and accelerated life testing was performed. The devices were subjected to three different stress conditions which are summarized in Table I. The experimental procedures for each test are summarized below.

Temperature stress test—A total of 73 unpackaged devices were stressed at 400°C in a dry N_2 ambient. The forward and reverse characteristics of all devices were checked periodically; the doping profiles of ~15 percent of the devices were also checked periodically. Only small changes were observed; typically, breakdown voltage changes were <8 percent. Samples from the population were taken at 80, 285, and 400 h, and then packaged for RF testing in the waveguide cavity. The RF performance of unstressed devices from each lot was also characterized in a waveguide cavity. The RF performance of the stressed population did not differ from that of the unstressed population.

Non-RF bias-temperature stress (BTS)—Seven packaged devices were biased to dissipate the same amount of power as dissipated when the devices were operated in the waveguide cavity at the peak efficiency point. The test fixture was purposely arranged so that the devices did not oscillate. The thermal impedance of the devices was measured to determine junction temperature [9]. The heat sink temperature was varied between 103 and 166°C during the test duration of 360 h. The devices were periodically checked; no significant changes in the RF or dc characteristics were observed. Upon failure (by catastrophic short circuit) devices were uncapped and were all recovered by a slight mesa etch suggesting that the predominant failure mechanism was related to surface rather than bulk effects. No surface passivation was applied to the devices reported here. The efficiencies of the recovered devices were measured and found to be essentially unchanged by the life test.

RF BTS Test—Ten free-running microstrip oscillator circuits such as shown in Fig. 3 were employed. All oscillators were thoroughly RF and dc characterized and their thermal impedances measured. Great care was taken to avoid contamination by the ambient. Provisions for measuring the output power of the oscillators at elevated heat-sink temperatures were included. The units were subjected to five stress steps of 500 h each at heat-sink temperatures of 25, 50, 75, 100, and 125°C. At all times the operating bias was adjusted to obtain maximum output power from each oscillator. At the end of each stress step, RF and dc characterizations were made with the heat sink at room temperature and the thermal impedance remeasured. As before, shorted devices were recovered by a slight mesa etch.

TABLE I
SUMMARY OF LOW–HIGH–LOW IMPATT RELIABILITY STUDIES

Stress Test	Stress Conditions	No. of Devices	MTTF (hrs)	Comments
Temperature	400 hrs at 400°C	73	2×10^{8}	V_B change<8%
Non-rf Bias Temperature	360 hrs at 103-166 C	7	8×10^{6}	Failure recovered by slight mesa etch
RF Bias-Temperature	500 hrs each at 25, 50, 75, 100 and 125 °C	10	5×10^{5}	V_B change~25% Chip tuning Recoverable.

*Assumes failure rate obeys the Arrhenius relationship. However under operating conditions hot carrier effects are dominant which results in a useful device life considerably less than that indicated above (see text).

The data from these tests were analyzed to determine the mean-time-to-failure (MTTF) for the GaAs IMPATT's assuming temperature effects to be dominant (i.e., the failure rate was assumed to obey the Arrhenius relationship). Based on the work of other investigators, an activation energy of 1.6 eV was assumed.

Table I shows the resulting MTTF's for the three different tests referenced to a normal operating junction temperature of 200°C. Note that the predicted MTTF resulting from the first test (temperature stress only) is considerably greater than the MTTF predicted from the last two in which current bias is also applied. This observation suggests that bias (specifically current stress), rather than temperature is the driving force limiting device reliability.

In another paper [9], a device model [3] is employed to establish a relationship between the change in device breakdown voltage and the change in avalanche zone width. By analyzing the RF BTS data, the change in junction position is found to be related to the current density J by

$$-\Delta X_p = k_j J t \tag{3}$$

where ΔX_p is the change in avalanche zone width, t is the time, and k_j is the current-related coefficient of proportionality. The mean value of k_j is found to be 0.072 Å/kA/cm²/h with a standard deviation of 0.018 for the ten devices. As suggested by (3), hot carrier effects are dominant while temperature effects assume a secondary role under normal operating conditions for the devices cited herein.

The value of k_j is sufficiently large to affect the reliability of fixed tuned electronic systems. In such applications, a total junction motion of ~300 Å will sufficiently change the characteristics of a Read-type IMPATT to require retuning so as to reoptimize the device-circuit interaction. For typical current densities of 3 kA/cm^2 for 15-GHz devices, this will occur in ~1500 h of operation.

Although the devices of this investigation are superior in terms of useful life to equivalent devices with no refractory barrier metal (wherein temperature stress alone will result in a medium life of about 1000 h), their reliability characteristics are nonetheless inadequate for long term space applications. Further reliability improvements are necessary and can be envisioned by employing implanted (or diffused) junctions [10], at the expense, however, of a more complicated fabrication procedure.

IV. FET Preamplifier

To obtain the first 40 dB of gain a six-stage FET preamplifier is employed. The GaAs FET's with electron beam defined gates were fabricated by a process developed previously for power devices [11]. The preamplifier is seen as the first chassis on the left in the photo of Fig. 2. Fig. 5 shows the preamplifier chassis fitted with SMA connectors for testing the first four stages. By changing a gold ribbon bond, the last two stages, or the entire six-stage preamplifier, can be tested prior to integration with the IMPATT driver and power amplifiers. The circuit design is based on the small signal S-parameters of FET's having 0.5-μm long electron beam defined gates. The first four stages employ 300-μm gatewidth devices while the last two use two 300-μm devices each. For the 300-μm chip the real part of the input and output impedance is about 10 Ω and 22 Ω, respectively. The maximum available gain for these devices at 15 GHz is typically 7 to 9 dB. Simple single section $\lambda/4$ transformers and bond wire inductance are used to achieve conjugate impedance matching at the design frequency. The FET's are mounted on gold discs and located in holes, 1 mm in diameter, drilled in the 0.25-mm thick alumina substrate. For dc blocking between stages, 10-pF beam lead capacitors are employed. Seen also in the photo of Fig. 5 are the gate and drain bias rf chokes ($\lambda/4$ sections of high and low impedance transmission lines) as well as the 10 dB backward coupler etched integrally on the alumina substrate at the far right of the preamplifier. The Schottky detector diode which activates the IMPATT shutdown circuit is mounted on the coupled arm of the coupler while the isolated arm is terminated in 50 Ω. The first four FET stages operate at a 4-V drain bias while the last two stages operate at 6 V. A voltage dropping resistor is used so as to power the entire six-stage preamplifier from a single drain power supply of 6 V.

Fig. 6 shows the measured gain compression curve for the FET preamplifier. A small signal gain of 42 dB and an output 1-dB gain compression point of 20 dBm is achieved. To assess the preamplifiers contribution to the third order distortion of the integrated amplifier, two-tone third order intermodulation measurements were made on the preamplifier alone. At an input level of −33 dBm for each tone (separated by 10 MHz) the output third order products are down 33 dB below the carrier level. An an input level of −23 dBm, the third order products are 12 dB below the carrier level. As shown in Section VI the preamplifiers contribution to the third order distortion is small to negligible compared to the distortion introduced by the IMPATT stages.

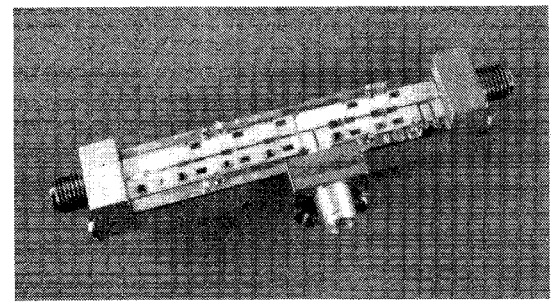


Fig. 5. FET preamplifier ready for testing.

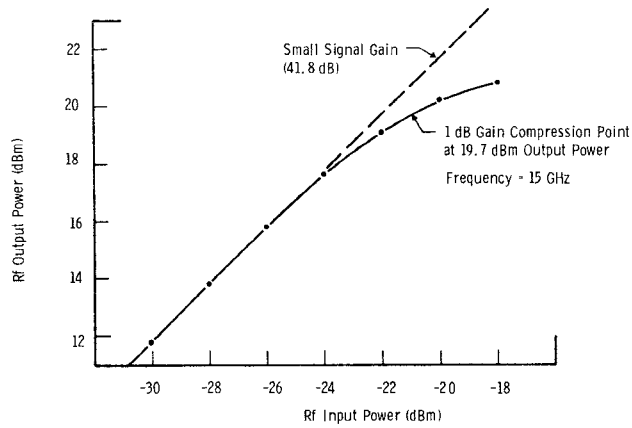


Fig. 6. Gain compression characteristic for 15-GHz six-stage preamplifier.

V. IMPATT Driver and Power Amplifier Stages

Although it is possible to develop high power stable GaAs IMPATT amplifiers (i.e., stable under zero RF drive) using flat profile IMPATT's, it is not practical to do so with amplifiers employing high efficiency GaAs IMPATT's with low–high–low doping profiles [12]–[15]. This is because for these diodes a large increase in negative resistance accompanies reduced rf drive levels, (however, a recent paper, [20] has suggested that the use of a molybdenum Schottky barrier contact can reduce this effect). As a consequence, an amplifier tuned for maximum output power at a high input drive level (i.e., the real part of the circuit impedance presented to the diode is low) will oscillate at reduced or zero drive levels (because the magnitude of the diode's negative resistance has increased to a value greater than the real part of the circuit impedance) [16]. For this reason, the low–high–low GaAs

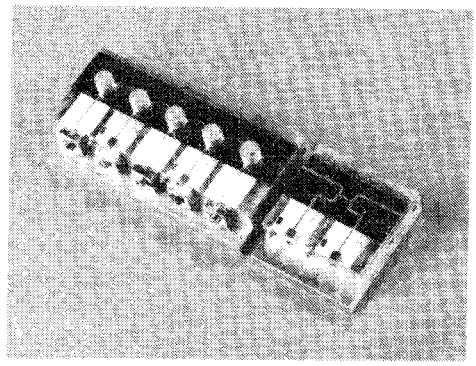


Fig. 7. IMPATT driver and balanced power amplifiers.

IMPATT's are much more appropriate for injection-locked oscillator (ILO) operation than for stable amplifier operation, provided the dynamic range and bandwidth requirements can be satisfied. To prevent spurious output and conserve prime power below threshold input levels, an IMPATT bias shutdown circuit can be incorporated as discussed previously. Furthermore, this type of power saturated amplifier is suitable for transmission of digital phase modulated signals such as BPSK or QPSK and is directly applicable to the spacecraft transmitter application [13]. Other advantages of the ILO approach include higher amplifier efficiency due to higher gain per stage, and improved overall amplifier gain stability with respect to changes in ambient temperature; this is because the gain variation due to temperature changes is primarily affected by the temperature characteristics of the final ILO stage rather than by the cumulative gain variation of all preceeding stages. Because of the above design considerations, the ILO approach is implemented in both the IMPATT drive and balanced power stages.

A. Driver Amplifier Design and Performance

The IMPATT driver amplifier consists of two stages of circulator-coupled reflection amplifiers operating in the ILO mode. Three additional MIC circulators serve as isolators at the input and output and between stages. The driver stage design follows closely that used previously at Texas Instruments for development of similar amplifiers [12]–[15]. The driver amplifier is shown as the chassis on the left in Fig. 7. The matching circuits are fabricated on 0.25-mm alumina substrates, while the circulator disks are etched on TTI-390 0.5-mm thick ferrite. SmCo permanent magnets mounted beneath the ferrite directly underneath the disk resonators bias the ferrite for circulator action. For additional control of the magnetic fringing field lines, and circulator optimization, iron "pucks" are placed on the top surface of the ferrite. The insertion loss for a single pass through any one circulator was measured to be about 0.4 dB while the adjacent port-to-port isolation is typically 20 dB.

The driver amplifier is designed to increase the power level to greater than 1 W over the input dynamic range, and yet maintain a locking bandwidth considerably in excess of 250 MHz to ensure the bandwidth performance

TABLE II
DRIVER STAGE PERFORMANCE

Input Power (dBm)	Locking Bandwidth (MHz)	Locking Limits (15 GHz+MHz)	Output Power (dBm)	Diode Operating Voltage and Current and 10 mA Breakdown Voltage	
				First Stage	Second Stage
+ 10	420	-160, + 260	31.0		
+ 15	820	-340, + 480	31.1	26 V, 147 mA	35 V, 211 mA
+ 20	1500	-660, + 840	31.2	V_B = 17 V	V_B = 23 V

Driver Stage Operating Voltage: 38V

Series Bias Resistors: First Stage - 82 Ω
Second Stage - 13.3 Ω

Total Dc Input Power: 13.6 W

Power-Added Efficiency: 10%

over temperature. Because the locking bandwidth for a single-stage ILO is nominally proportional to the square root of the input power, the critical design operating point occurs at the lower input levels. For an input to the driver amplifier of + 10 dBm the intrinsic gain of the first stage IMPATT is 17.8 dB with 26.7-dBm output power, while the second stage IMPATT yields a gain of 6.4 dB and an output power of 32.0 dBm. The actual measured driver amplifier gain is only 21 dB, because of circulator (0.4 dB) losses. Both stages employ the same circuit as used for the oscillator test fixture. Tuning with metallized ceramic chips is done under RF drive conditions and optimized for maximum output power. The resultant load resistance is only slightly higher from that required for optimized free oscillator operation since the gain is high (especially for the case of the first stage IMPATT) [17]–[18]. The locking bandwidth can be estimated from the external, Q_e, as

$$\Delta f = \frac{2f_o}{Q_e}\left(\frac{1}{G}\right)^{1/2}$$

For the first stage, assuming a Q_e of about 8 (as estimated in Section IV-B with $L-0.2$ nH) Δf is 483 MHz. A locking bandwidth of 420 MHz was actually measured. For the second stage the locking bandwidth is much greater since the gain is lower. Consequently the first stage of the driver determines the locking bandwidth of the entire amplifier.

Table II summarizes the driver amplifier's performance, as well as the operating characteristics of the actual diodes used. An output power of 1.3 W and a power-added efficiency of 10 percent were achieved for the amplifier, including the losses in the series bias resistors. These resistors are necessary to stabilize the IMPATT's against low-frequency bias oscillations.

Although a 10-percent power-added efficiency was realized for this amplifier, a more careful pairing up of diodes, so that the operating voltage of both would be closer to the 35-V value, would result in still higher efficiency, since less power would be dissipated in the series bias resistors.

B. Balanced Power Amplifier Design and Performance.

A 3-dB microstrip interdigital hybrid coupler, the so-called Lange coupler [19], is used to power-combine the

TABLE III
BALANCED STAGE PERFORMANCE

Input Power	Output Power	Gain	Dc Input Power Diode A	Dc Input Power Diode B
31 dBm	36 2 dBm	5 2 dB	35 5 V, 279 mA	35 4 V, 242 mA

Power-Added Efficiency 16%

Center Frequency ~15 GHz

Locking Bandwidth 1 5 GHz

Operating Characteristics of Diode B as a Free-Running Microstrip Oscillator

10 mA Breakdown Voltage 23 6 V
Operating Voltage Current 35 V, 224 mA
Frequency 15 6 GHz
Output Power 32 5 dBm (1 8 W)
Dc-to-rf Efficiency 23%

outputs of two IMPATT diodes as shown schematically in Fig. 1. Both the coupled and the direct ports of the coupler are terminated with an identical matching circuit and diode combination. Ideally, the voltage reflection coefficients looking into the diode circuits are equal in both magnitude and phase. Because of the 90° phase properties of the hybrid, the two reflected waves add in phase at the normally isolated port and cancel at the input port. For lower loss, fused quartz (0.25 mm thick) is used as the substrate for the coupler fabrication. A loss of between 0.25 and 0.3 dB for a single pass through the coupler over and above the nominal 3-dB power split is measured at 15 GHz. Although the balanced stage avoids the use of magnets and ferrite material, in actual practice an external output isolator would be desirable to avoid load-pulling effects. This is because the 3-dB coupler does not isolate the diodes from reflected power due to mismatched loads.

Fig. 7 shows the balanced power stage (minus the IMPATT diodes) alongside the driver chassis prior to final assembly and tuning. Also shown in the photograph is the K_u-band Lange coupler etched on a $22.5\times10\times0.25$ mm fused quartz substrate. The matching circuits consisting of the single section $\lambda/4$ transformer, tuning pads, and 50-Ω line are all fabricated on the $7.5\times7.5\times0.25$ mm alumina substrate.

Tuning of the balanced stage begins with careful selection of a pair of diodes. Diodes are selected to have similar breakdown and operating voltages, power output, and frequency of operation when tested in the microstrip oscillator circuit. The pair of diodes is then simultaneously tuned in the balanced stage to realize maximum combined output power from the output port of the coupler, with a nominal input power of 31 dBm. As in the case of the driver stage, both diodes are single mesa devices that operate in the injection-locked oscillator mode. However, since the driver stage output power stays nearly the same at 31 dBm, the balanced stage locking bandwidth is determined by this one input level. That is, the gain of the balanced stage (and hence the locking bandwidth) remains constant at about 5 dB.

Table III shows the balanced stage performance. An output power of 4.2 W at a gain of 5.2 dB and an intrinsic

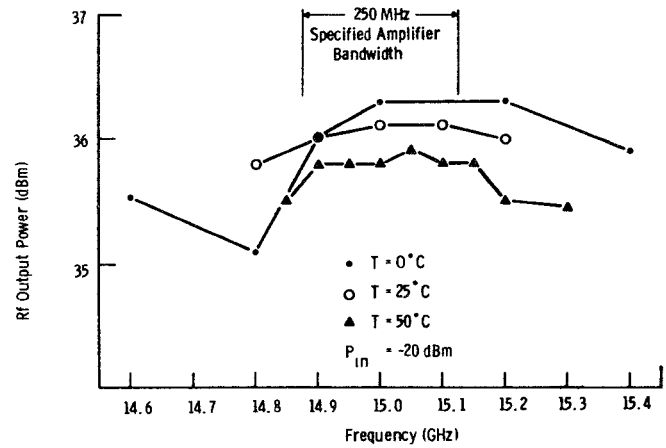


Fig. 8. Output power versus frequency characteristic for 4-W integrated amplifier.

power-added efficiency of 16 percent was achieved at 15 GHz. A locking bandwidth of about 1.5 GHz was obtained. The operating characteristics of one of the diodes in the microstrip oscillator test fixture are listed at the bottom of the table. This diode yielded 1.8 W at an efficiency of 23 percent at 15.6 GHz. The second diode had nearly the same characteristic, with slightly less dc-to-RF efficiency (~20 percent).

In the final incorporation of the balanced stage into the integrated amplifier, series resistors are used to bias the two diodes from a 38-V dc source. A 9 and an 11-Ω resistor are employed.

VI. Integrated Amplifier Performance

Fig. 8 shows the RF output power of the integrated amplifier over the specified frequency band of 15 GHz ± 125 MHz at three temperatures, 0, 25, and 50°C. The output power is seen to vary no more that 0.5 dB for any frequency within the band over the 0 to 50°C range. Over the input range of −30 to −20 dBm the output power varies less than 0.2 dB at 15-GHz for all three temperatures measured. No spurious signals were observed in the specified operating bandwidth within 50 dB of the carrier signal. Third-order intermodulation tests measured over the input dynamic range revealed third order products within 8 to 10 dB of the two equal magnitude carrier signals ($\Delta f = 10$ MHz) at a total output power of 4 W. This distortion is primarily due to the large signal, nonlinear, operation of the IMPATT stages (it may be noted that power FET's operated in the fully power saturated mode yield similar third order products and are typically 10 dB below the carrier level). The AM to PM conversion was measured at 14.9, 15.0, and 15.1 GHz over the 10-dB input dynamic range. The worst case AM–PM conversion is 4.5°/dB. The overall dc to RF efficiency including all bias circuit losses is 10.8 percent.

VII. Conclusions

The realization of the 15-GHz, 4-W 56-dB gain microstrip amplifier using GaAs FET's and Schottky–Read IMPATT diodes demonstrates the advantages of utilizing

both types of devices in an integrated power amplifier. The 40-dB gain FET preamplifier employs simple-cost-effective circuitry and provides truly stable preamplifier operation. The IMPATT driver and balanced power stages, utilizing a total of four single mesa diodes operating in the ILO mode, provide an output power of 4 W with as much as 26-dB gain and 400 MHz locking bandwidth at mid *Ku*-band.

A TiW barrier layer to retard device degradation due to semiconductor-intermetallic reactions at the Schottky junction is incorporated in the IMPATT diodes to improve reliability. Although the reliability of these devices is greatly enhanced over similar devices having no barrier metallization, results obtained from extensive accelerated life tests indicates that device degradation does occur and is current, rather than temperature stress, induced.

The small size (220 cm^3), light weight (444 g), overall dc to RF conversion efficiency (10.8 percent), output power stability with changes in temperature (<0.5 dB over 0 to 50°C), and potential reliability of the integrated amplifier (higher device reliability must still be established) makes it feasible for use in airborne and spacecraft transmitter applications.

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